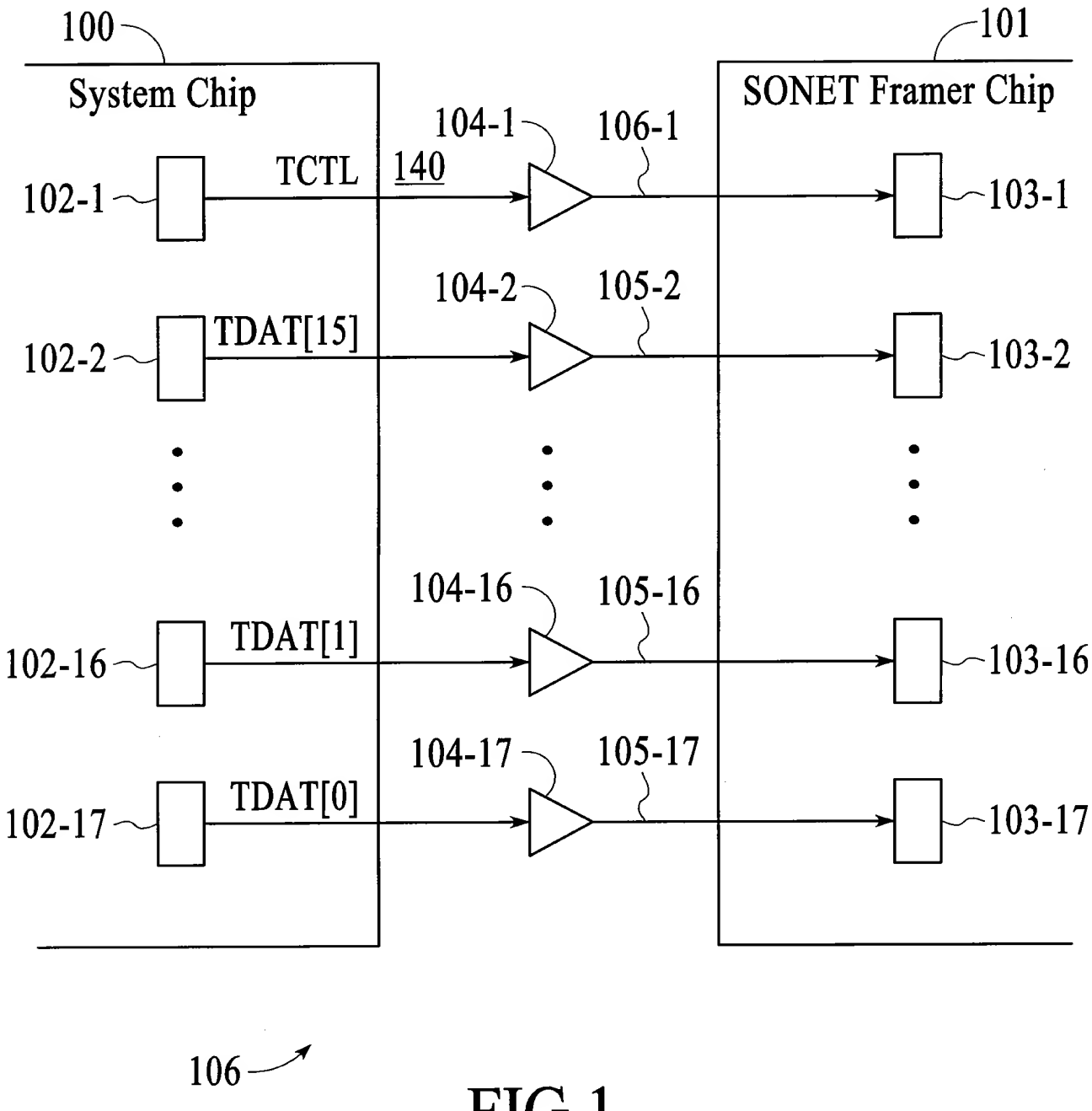
100
System Chip
101
SONET Framer Chip
104-1
106-1
TCTL
140
102-1
103-1
104-2
105-2
TDAT[15]
102-2
103-2
104-16
105-16
TDAT[1]
102-16
103-16
104-17
105-17
TDAT[0]
102-17
103-17
106

FIG.1

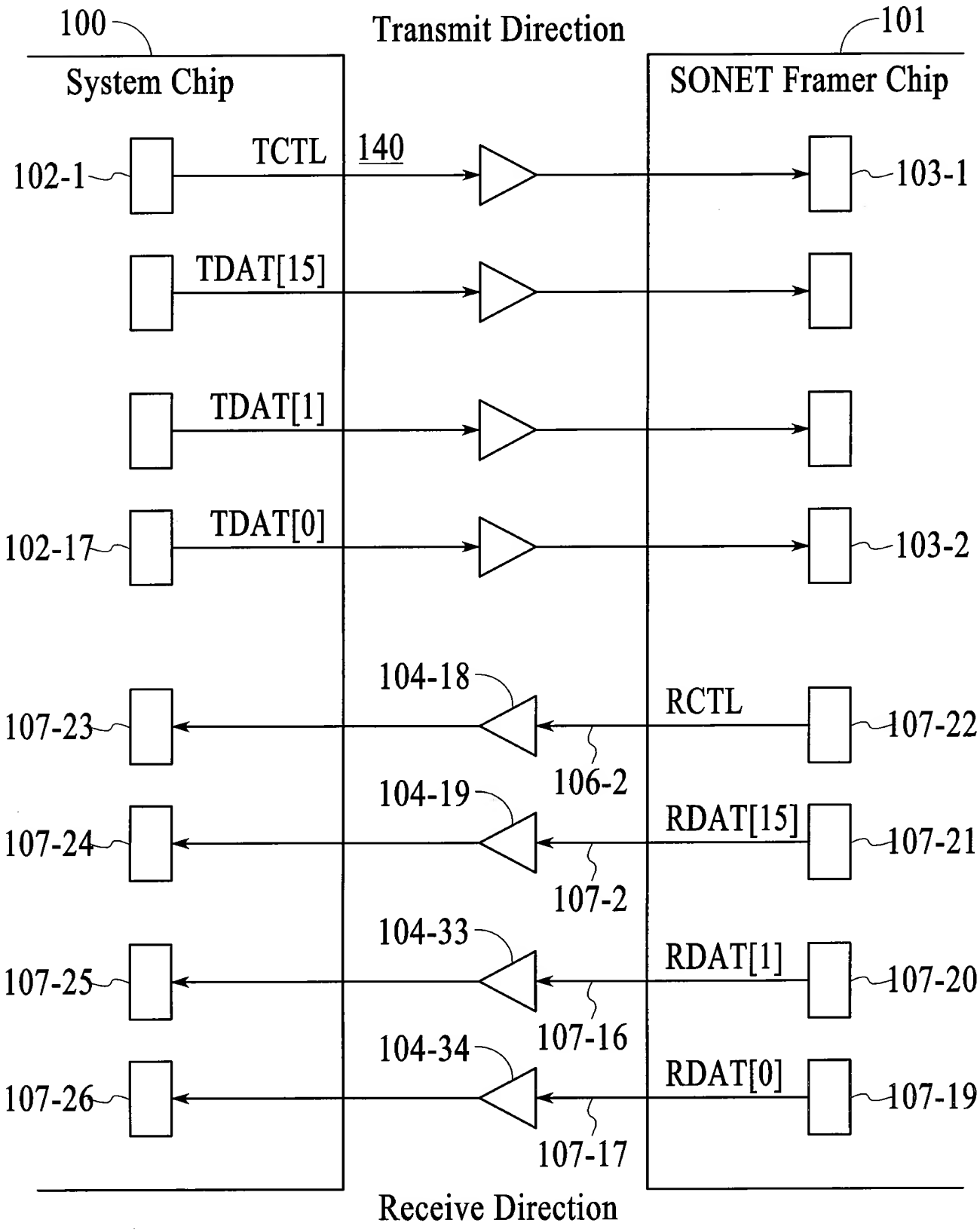
100
System Chip
Transmit Direction
101
SONET Framer Chip
102-1
TCTL
140
103-1
TDAT[15]
TDAT[1]
102-17
TDAT[0]
103-2
104-18
RCTL
107-23
107-22
106-2
104-19
RDAT[15]
107-24
107-21
107-2
104-33
RDAT[1]
107-25
107-20
107-16
104-34
RDAT[0]
107-26
107-19
107-17
Receive Direction
106

FIG.1A

200

Cycle	Tctl	TDAT[1]															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	X	X	0	0	0	0	0	0	0	0	0	A	B	C	D
2	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
3	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
6	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
8	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
12	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
13	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
15	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
16	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
18	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
202 19	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
21	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−18	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−17	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−16	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−15	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−14	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−13	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−12	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−8	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−7	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−5	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−4	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−3	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−2	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α+1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

FIG.2

300

Cycle	Tctl	TDAT[1]															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	X	X	0	0	0	0	0	0	0	0	0	A	B	C	D
2	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
3	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
6	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
8	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
12	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
13	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
15	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
16	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
18	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
19	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
21	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
20α−18	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−17	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−16	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−15	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−14	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−13	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−12	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−9	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
20α−8	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−7	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−5	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−4	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−3	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−2	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α+1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0

FIG.3

400

Cycle	Tctl	TDAT[1]															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	X	X	0	0	0	0	0	0	0	0	0	A	B	C	D
2	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
3	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
6	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
8	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
12	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
13	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
15	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
16	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
18	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
19	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
21	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−18	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
20α−17	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−16	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−15	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−14	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−13	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−12	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−8	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
20α−7	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−5	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−4	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−3	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−2	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α+1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

FIG.4

500

Cycle	Tctl	TDAT[1]															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	X	X	0	0	0	0	0	0	0	0	0	A	B	C	D
2	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
3	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
5	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
6	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
8	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
9	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
12	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
13	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
15	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
16	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
18	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
19	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
21	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
20α−18	1	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1
20α−17	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−16	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−15	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−14	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−13	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−12	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−11	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−10	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
20α−9	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
20α−8	0	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
20α−7	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−5	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−4	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−3	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−2	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α−1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
20α+1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0

FIG.5

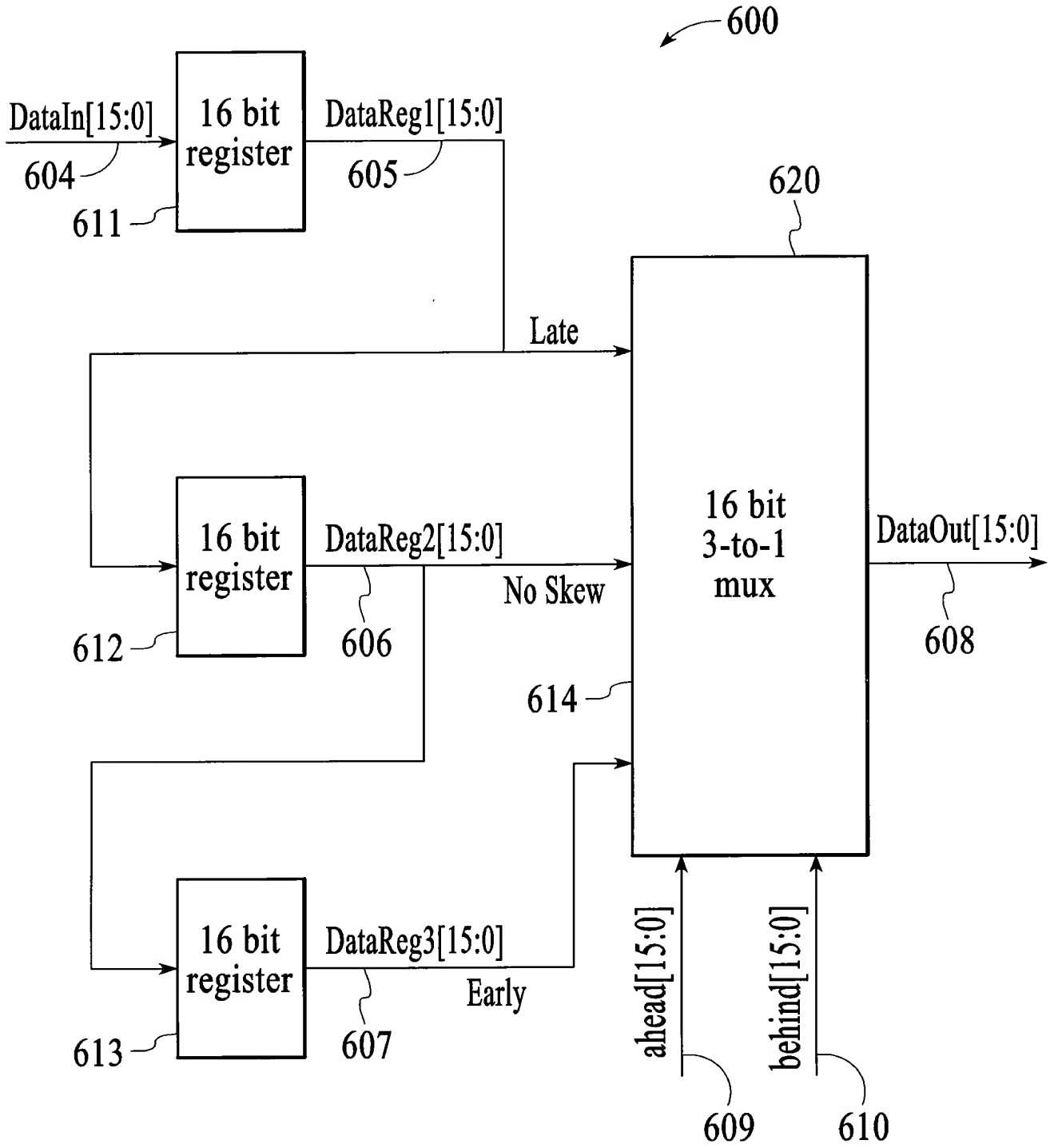
600
DataIn[15:0]
604
16 bit
register
611
DataReg1[15:0]
605
620
Late
16 bit
register
612
DataReg2[15:0]
606
No Skew
16 bit
3-to-1
mux
DataOut[15:0]
608
614
16 bit
register
613
DataReg3[15:0]
607
Early
ahead[15:0]
609
behind[15:0]
610

FIG.6

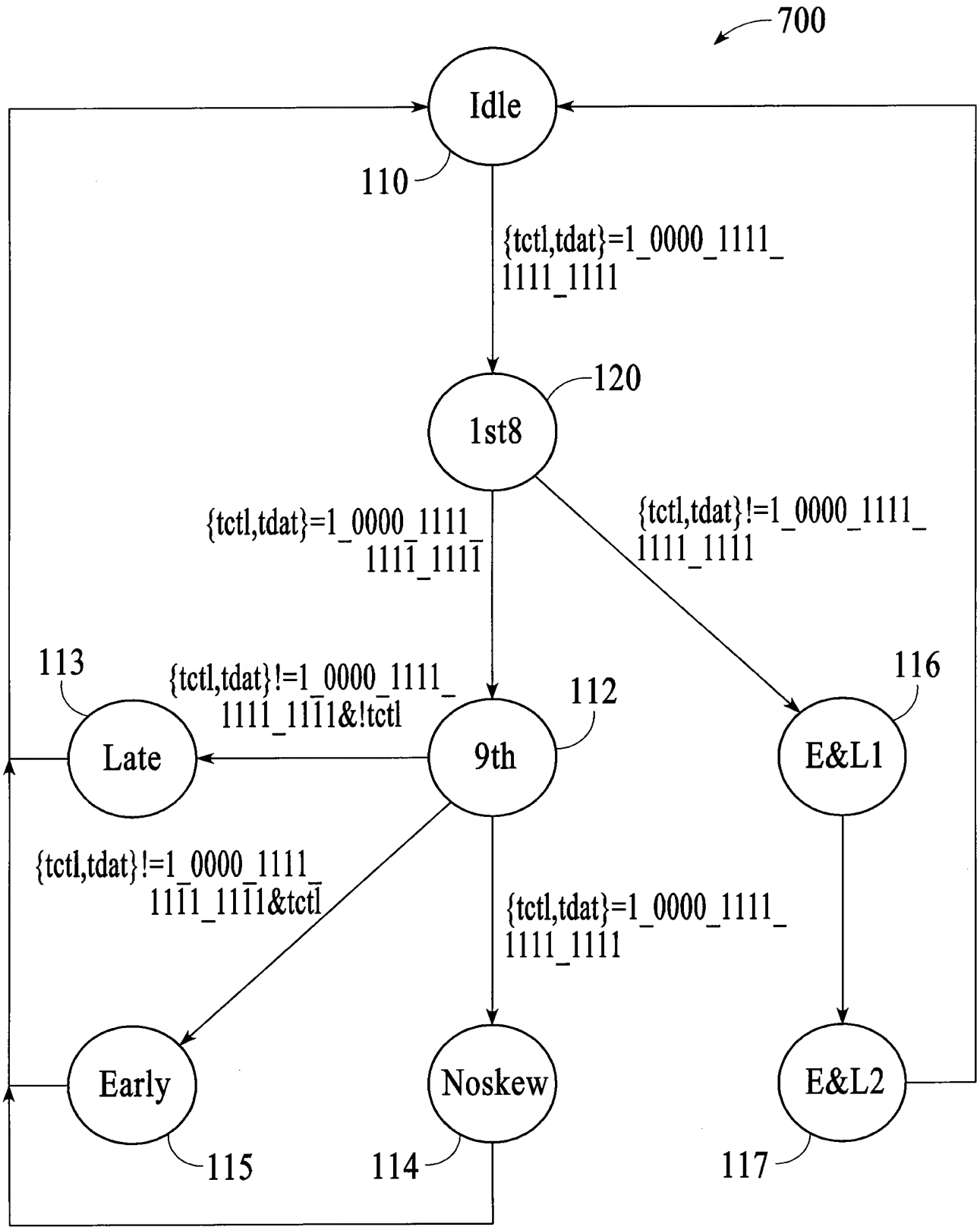
700
Idle
110
{tctl,tdat}=1_0000_1111_
1111_1111
120
1st8
{tctl,tdat}=1_0000_1111_
1111_1111
{tctl,tdat}!=1_0000_1111_
1111_1111
113
{tctl,tdat}!=1_0000_1111_
1111_1111&!tctl
112
116
Late
9th
E&L1
{tctl,tdat}!=1_0000_1111_
1111_1111&tctl
{tctl,tdat}=1_0000_1111_
1111_1111
Early
Noskew
E&L2
115
114
117

FIG.7

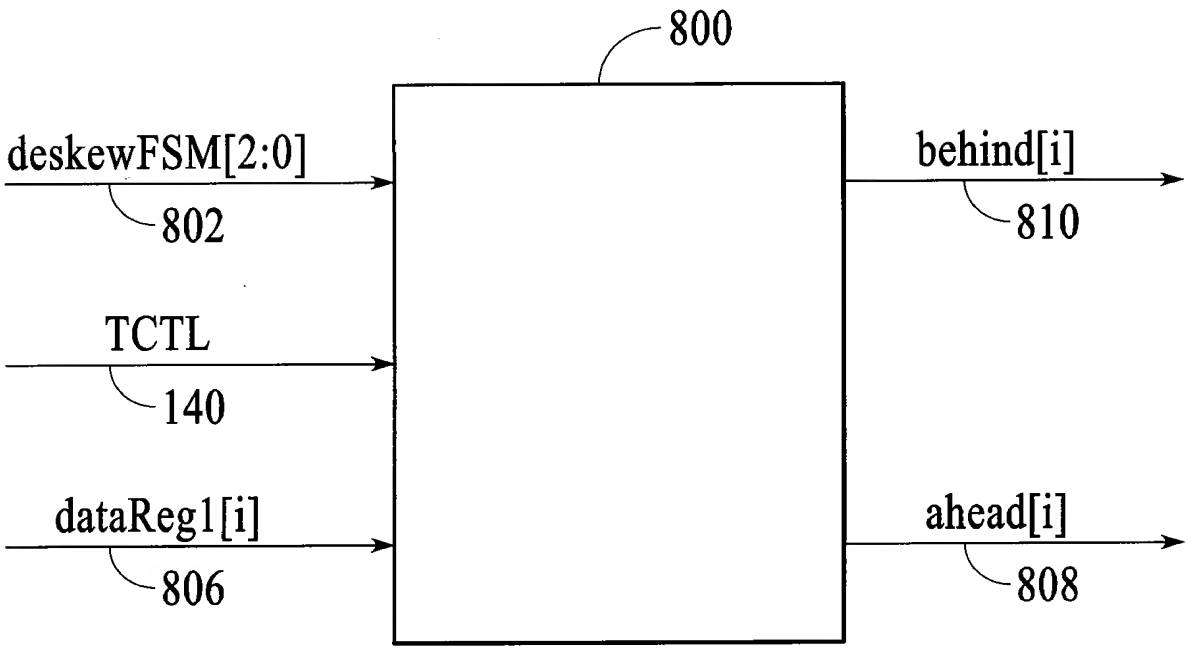
800
deskewFSM[2:0]
802
TCTL
140
dataReg1[i]
806
behind[i]
810
ahead[i]
808

FIG.8

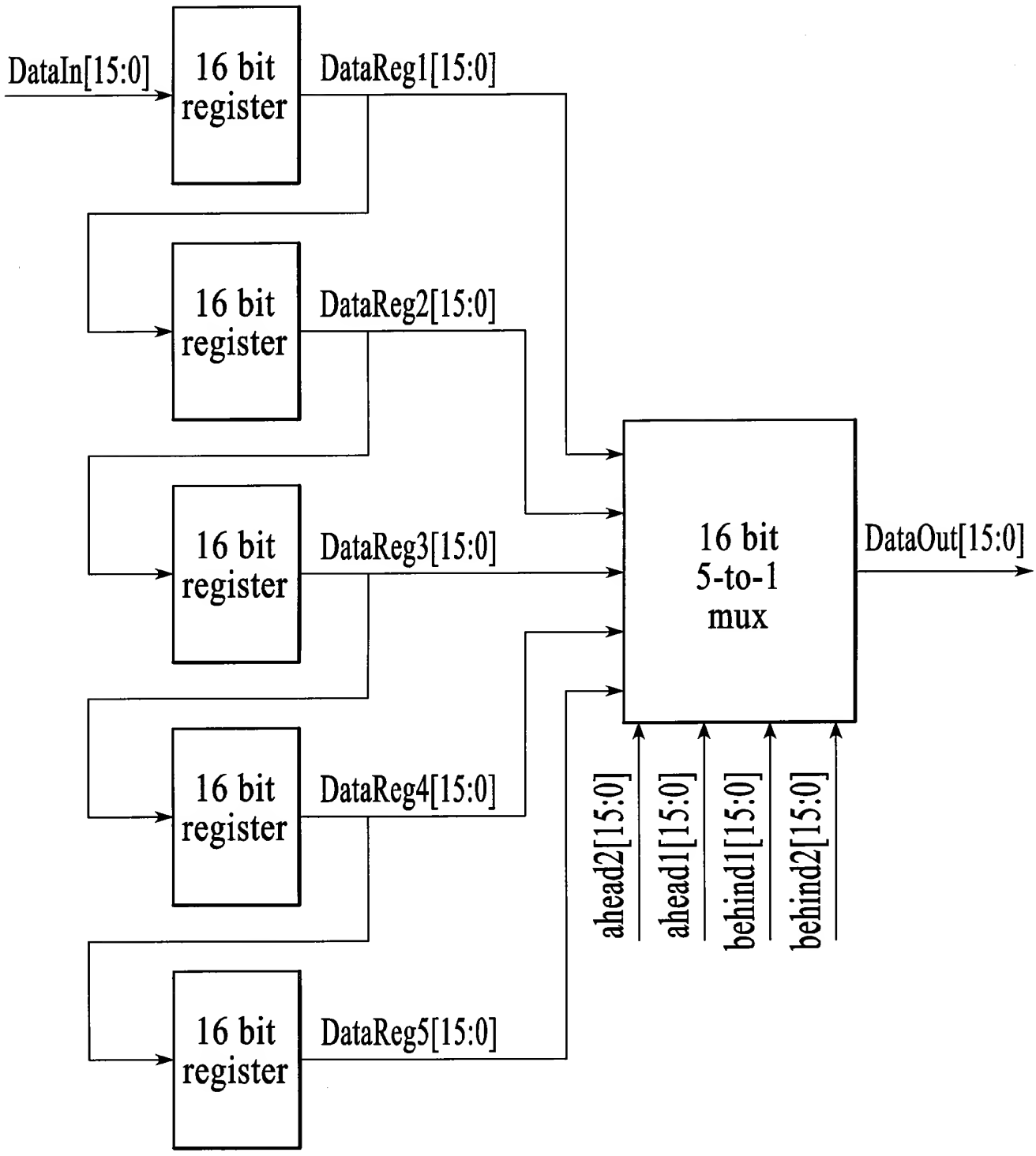
DataIn[15:0]
16 bit register
DataReg1[15:0]
16 bit register
DataReg2[15:0]
16 bit register
DataReg3[15:0]
16 bit register
DataReg4[15:0]
16 bit register
DataReg5[15:0]
16 bit 5-to-1 mux
DataOut[15:0]
ahead2[15:0]
ahead1[15:0]
behind1[15:0]
behind2[15:0]

FIG.9

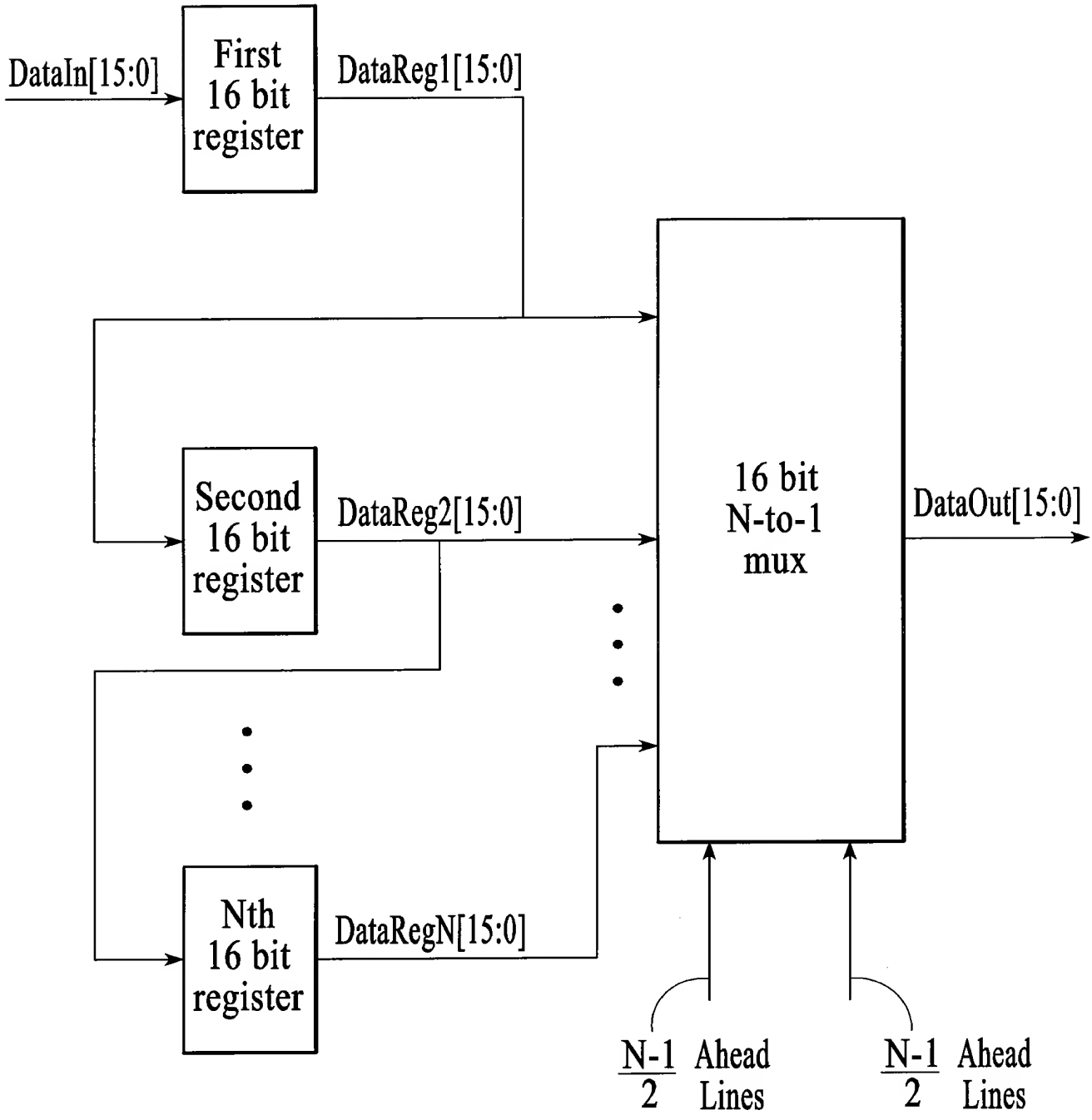
DataIn[15:0]
First
16 bit
register
DataReg1[15:0]
Second
16 bit
register
DataReg2[15:0]
Nth
16 bit
register
DataRegN[15:0]
16 bit
N-to-1
mux
DataOut[15:0]
N-1 Ahead
2 Lines
N-1 Ahead
2 Lines

FIG.10